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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/375,328	08/17/1999	AHMAD R. ANSARI	M-7669-US	4890

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EXAMINER
KISS, ERIC B

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 12/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/375,328	ANSARI, AHMAD R.	
	Examiner	Art Unit	
	Eric B. Kiss	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 41-52* is/are pending in the application.

4a) Of the above claim(s) *41-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *03 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed December 3, 2002 has been received and entered. Claims 1-30 and 41-52 are pending.

Election/Restrictions

2. During a telephone conversation with Eric Stephenson (Reg. No. 38321) on August 16, 2002 a provisional election was made without traverse to prosecute the invention of group 1, claims 1-30. Claims 31-40 were withdrawn from further consideration by the examiner in a prior office action, as being drawn to a non-elected invention (See 37 CFR 1.142(b)) based on the following requirement:

Restriction to one of the following inventions was required under 35 U.S.C. 121:

I. Claims 1-13, drawn to a general method of using vector transfer instructions, classified in class 717, subclass 114+.

II. Claims 14-30, drawn to a general data processing system implemented with a set of vector transfer instructions.

III. Claims 31-40, drawn to a general compiler for generating vector transfer instructions, classified in class 717, subclass 140+.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and III are related as process of using and process of making the product of group II (a set of vector transfer instructions). The use as claimed cannot be practiced with a materially different product. Since the product is not allowable, restriction is proper between said method of making and method of using. The product claim will be examined along with the elected invention (See MPEP § 806.05(i)).

3. Applicants affirmed the election of group 1, and cancelled the non-elected claims of group 3, claims 31-40 (See MPEP § 818.02(c)).

Claim 41, added by Applicants' amendment is drawn to non-elected group III, in that it involves the scheduling and/or generation of instructions by a compiler.

Claims 42-52, added by Applicants' amendment are drawn to non-elected group III, in that they involve the scheduling and/or generation of instructions by a compiler.

Accordingly, claims 41-52 are withdrawn from further consideration by the examiner as being drawn to a non-elected invention (See 37 CFR 1.142(b)).

Drawings

4. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on December 3, 2002, has been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

The Patent and Trademark Office no longer makes drawing changes. See 1017 O.G. 4.

It is applicant's responsibility to ensure that the drawings are corrected. Corrections must be made in accordance with the instructions below.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.185(a). Failure to take corrective action within the set (or extended) period will result in **ABANDONMENT** of the application.

Response to Amendment

5. Applicants' amendment to the specification appropriately addresses the objections to the drawings (those objections not otherwise addressed by the proposed drawing correction) and specification due to informalities as cited in the prior office action. Accordingly, these objections are withdrawn in view of Applicants' amendment.

Response to Arguments

6. In the third paragraph on page 12, Applicants argue:

> In contrast, in amended claims 1 and 14, Applicants claim at least one vector data instruction for transferring the vector data directly between a memory and a vector buffer. In the cited sections, neither Inagami nor Mohamed teaches at least one vector data instruction for transferring the vector data directly between a memory and a vector buffer.

However, as cited in the prior office action, Inagami discloses at least one vector data instruction for transferring the vector data directly between a memory and a vector buffer (see Fig. 4b, VL and VST instructions).

VL and VST are described as VECTOR LOAD and VECTOR STORE instructions, respectively (see NOTES section of Fig. 4b). Each of these instructions takes three arguments, namely a VECTOR REGISTER (VR), a VECTOR BASE REGISTER (VBR), and a VECTOR INCREMENT REGISTER (VIR). Each vector register is designed to hold vector data for subsequent processing (see column 5, lines 61-64; and Fig. 4b, VEA, VSM, and VEM instructions), and can therefore be considered vector buffers in the context of the relevant art.

The vector base registers and vector increment registers hold address information necessary for the transfer of vector data directly to/from specific memory locations (see column 6, lines 11-14). Therefore, the Examiner maintains that Inagami discloses at least one vector data instruction for transferring the vector data directly between a memory and a vector buffer.

Similarly, as cited in the prior office action, Mohamed discloses at least one vector data instruction for transferring the vector data directly between a memory and a vector buffer (see column 4, lines 20-34).

The vector load instruction (VL.w) of Mohamed functions in the same manner as that of Inagami, with the following differences illustrated in the sample source code provided in column 3, line 60 through column 4, line 19: the vector base address is first loaded into a scalar register (analogous to Inagami's vector base register) using a VLI.w instruction (see column 3, lines 63-64; and column 4, line 10); and an immediate value offset ("#" followed by an integer) is used as the third argument to the vector load instruction to complete the address information (analogous to Inagami's vector increment register). However, the results are similar, namely, vector data is loaded directly from particular memory locations into vector registers (vector buffers) for subsequent processing. Therefore, the Examiner maintains that Mohamed discloses at least one vector data instruction for transferring the vector data directly between a memory and a vector buffer.

7. In the last paragraph on page 12, Applicants argue:

> However, because claims 27 and 28 depend from claim 14, and because claim 14 has been shown to be patentably distinguishable from Inagami, claim[s] 14, 27, and 28 are patentably distinguishable from Inagami in view of Booth for at least these same reasons.

In response to Applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Furthermore, whereas Applicants' arguments allege that claims 14, 27, and 28 are patentably distinguishable from Inagami in view of Booth, claims 14, 27, and 28, were rejected as being unpatentable over Booth in view of Inagami. Applicants' arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which the Applicants think the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-11, 14-23, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,803,620 to Inagami et al.

As per claim 1, Inagami discloses a method for identifying use of vector data (see Fig. 2, EXVP instruction description) and implementing at least one instruction for transferring vector data between a memory and a vector buffer accessible by a processor (see Fig. 4b, VL and VST instructions).

As per claim 2, Inagami further discloses implementing a synchronization instruction to synchronize accessing and processing vector data (see column 10, lines 15-25).

As per claim 14, Inagami discloses a data processing system (see Fig. 1) comprising a cache (Fig. 1, item 31), a register file (registers; Fig. 1, item 32), and a vector buffer (vector registers; Fig. 1, item 41), including means for identifying use of vector data (see Fig. 2, EXVP instruction description), at least one instruction for transferring vector data between a memory and a buffer (vector register) accessible by a processor (see Fig. 4b, VL and VST instructions), and a synchronization instruction to synchronize accessing and processing vector data (see column 10, lines 15-25).

As per claims 3, 4, 15, and 16, Inagami further discloses a method and data processing system (see Fig. 1) including instructions for transferring data from the memory to the buffer (vector register) and from the buffer (vector register) to the memory (see Fig. 4b, VL and VST instructions, respectively).

As per claims 5, 6, 17, and 18, Inagami further discloses a method and data processing system (see Fig. 1) including instructions for transferring data from the general-purpose register to the buffer (scalar register in vector processing unit) and from the buffer (scalar register in

vector processing unit) to a general-purpose register (see Fig. 2, MVSG and MVGS instructions, respectively).

As per claims 7 and 19, Inagami further discloses a method and data processing system (see Fig. 1) including at least one instruction for determining whether the buffer is available for use (see column 10, lines 15-25).

As per claims 8-11 and 20-23, Inagami further discloses a method and data processing system (see Fig. 1) with vector instructions that include information about the starting address, length, and stride of a vector stream and the starting address of the buffer (vector register identifier) (see column 6, lines 11-42 and Fig. 4b).

As per claim 26, Inagami further discloses a data processing system containing a vector transfer unit (vector processing mechanism) operable to perform burst transfers of the vector data based on at lease one instruction (see column 1, lines 32-35).

10. Claims 1, 12-14, 24, 25, 27, 29, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,016,395 to Mohamed.

As per claims 1 and 14, Mohamed discloses a method and data processing system (see Fig. 3) comprising a cache (Fig. 3, item 330), a register file (scalar registers; see for example, column 20, line 64 through column 21, line 18), and a vector buffer (vector registers; see column 4, lines 20-24), including means for identifying use of vector data (see Fig. 2), at least one instruction for transferring vector data directly between a memory and a vector buffer (vector register) accessible by a processor (see column 4, lines 20-34), and a synchronization instruction

to synchronize accessing and processing vector data (see column 19, lines 18-28). Mohamed further discloses

As per claims 12, 13, 24, and 25, Mohamed further discloses a method and data processing system (see Fig. 3) with instructions including information indicating width of the vector data and whether the vector data is integer or floating point type (see column 3, lines 22-39 and column 11, lines 23 and 24).

As per claims 27, 29 and 30, Mohamed further discloses a data processing system (see Fig. 3) wherein a compiler identifies the use of vector data in a program that contains a vector data indicator (VIVID instruction) and implements at least one vector transfer instruction when the compiler recognizes the vector data indicator (see column 3, lines 1-15).

Claim Rejections - 35 USC § 103

11. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

12. Claims 14, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,247,696 to Booth in view of Inagami.

Booth discloses with such a data processing system (see Fig. 1) comprising a cache (instruction buffer 22; see column 6, lines 23-26), a register file (scalar registers 16), and a vector buffer (vector registers 14), including means for identifying use of vector data (see column 5, lines 35-44), at least one instruction for transferring vector data between a memory and a buffer

accessible by a processor (see column 6, lines 27-39). Booth further teaches a compiler identifying the use of vector data based on whether the data is used in a program loop (see column 5, lines 35-44). Booth fails to teach a synchronization instruction to synchronize accessing and processing vector data. However, Inagami teaches implementing a synchronization instruction to synchronize accessing and processing vector data (see column 10, lines 15-25). Therefore, it would have been obvious to one having ordinary skill in the computer art at the time the invention was made to modify the system of Booth by adding a synchronization instruction as once taught by Inagami. One would be motivated to do so to allow for signaling to a processor that a vector read/write operation had been completed, marking the vector data valid and usable by the processor.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Kiss whose telephone number is (703) 305-7737. The examiner can normally be reached on Tue. - Fri., 7:30 am - 5:00 pm. The examiner can also be reached on alternate Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Morse can be reached on (703) 308-4789.

Any response to this action should be mailed to:
Commissioner of Patents and Trademarks
Washington, DC 20231
Or faxed to:
(703) 746-7239 (for formal communications intended for entry)
Or:
(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, 22202, Fourth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

EBK
December 19, 2002

ANIL KHATRI
PRIMARY EXAMINER